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2	BRS	12	circuit same latency same loop and (hdl or vhd)	USPAT; US-PGPUB	2003/05/08 14:10
3	BRS	7	circuit same latency same loop and (hdl or vhd)	USPAT; DERWENT	2003/05/08 14:08
4	BRS	64	circuit same delay same loop and (hdl or vhd)	USPAT; DERWENT	2003/05/08 14:10
5	BRS	10	circuit same delay same loop and (hdl or vhd) and pipeline	USPAT; DERWENT	2003/05/08 14:11

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6	BRS	5	lock same step same consistency same check	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
7	BRS	593	lock same step same controller and code	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
8	BRS	41	lock same step same controller and code and emulator	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
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1994 , Grenoble, France

A VHDL-based design methodology: the design experience of a high performance ASIC chip

Authors

Maurizio Valle
Daniele Caviglia
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Giovanni Nateri
Luciano Briozzo

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SIGDA : ACM Special Interest Group on Design Automation

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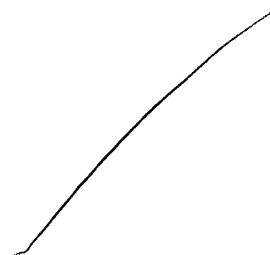
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1994 , Grenoble, France

Scheduling of behavioral VHDL by retiming techniques

Authors

N. Wehn
J. Biesenack
Peter Duzy
T. Langmaier
M. Münch
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S. Rumler

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Pages: 546 - 551 Series-Proceeding-Article


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1991 , San Francisco, California, United States

Scheduling for functional pipelining and loop winding

Authors

Cheng-Tsung Hwang
Yu-Chin Hsu
Youn-Long Lin

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SIGDA : ACM Special Interest Group on Design Automation
IEEE-CS : Computer Society


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ACM Press New York, NY, USA

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1992 , Anaheim, California, United States

High-level synthesis from VHDL with exact timing constraints

Authors

A. Stoll
P. Duzy

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EDAC : Electronic Design Automation Consortium
IEEE-CS : Computer Society
IEEE-CAS : Circuits & Systems
SIGDA : ACM Special Interest Group on Design Automation

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CHOP: A constraint-driven system-level partitioner

Authors

Kayhan Kükçakar
Alice C. Parker

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SIGDA : ACM Special Interest Group on Design Automation
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1 A formal approach to the scheduling problem in high level synthesis*Hwang, C.-T.; Lee, J.-H.; Hsu, Y.-C.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 10 Issue: 4 , Apr 1991

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1 Generating pipelined datapaths using reduction techniques to shorten critical paths*Lobo, D.A.; Pangrle, B.M.;*

Design Automation Conference, 1992. EURO-VHDL '92, EURO-DAC '92. European, 7-10 Sep 1992

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Design & Test of Computers, IEEE , Volume: 8 Issue: 1 , Mar 1991

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Computer Design: VLSI in Computers and Processors, 1990. ICCD '90. Proceedings., 1990 IEEE International Conference on , 17-19 Sep 1990

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Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceedings., 1993 IEEE International Conference on , 3-6 Oct 1993

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Design Automation Conference, 1992. EURO-VHDL '92, EURO-DAC '92. European, 7-10 Sep 1992

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efficient debugging of timing constraint violations
Ali Dasdan
Proceedings of the tenth international symposium on
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ACM Transactions on Design Automation of Electronic Systems (TODAES) October 2002
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TI: **VHDL for High-Level Synthesis of Digital Systems**

Source: Proceedings of conference as follows from Dialog 165, Eventline:

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EVENT DATE(S): September 4-7, 1990

HOST SITE: Inst. Mediterranee de Techn.

EVENT CITY: Marseille

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